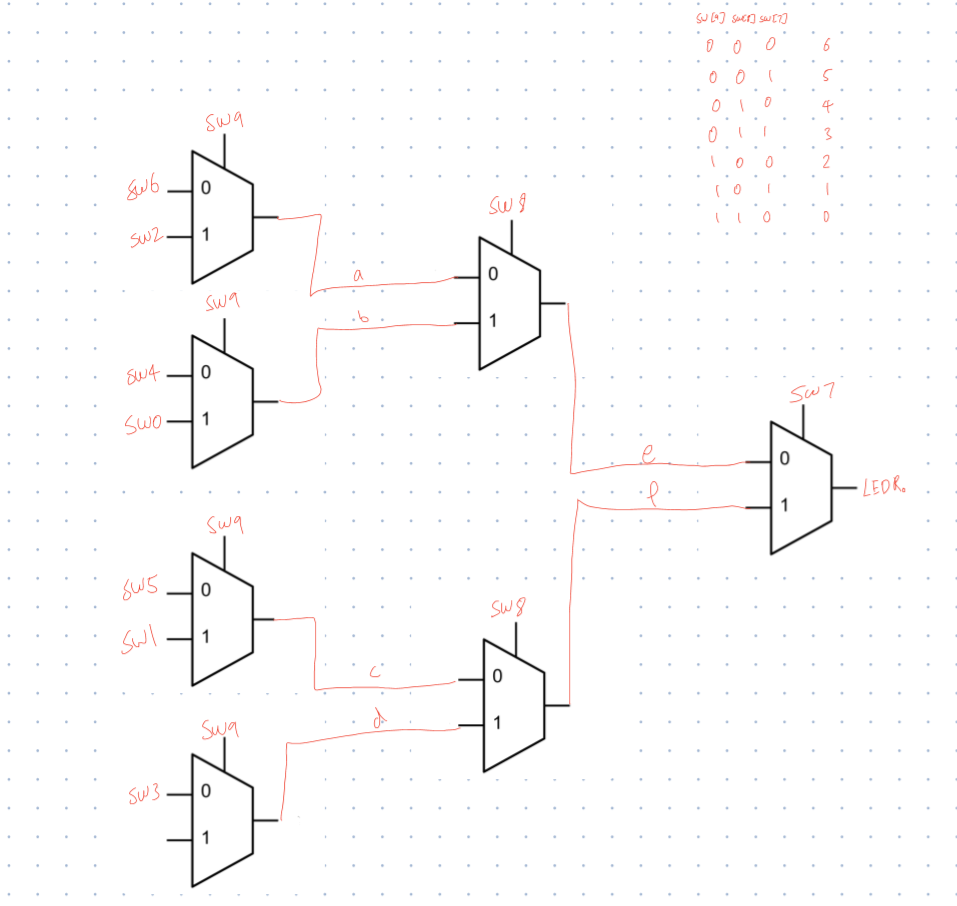
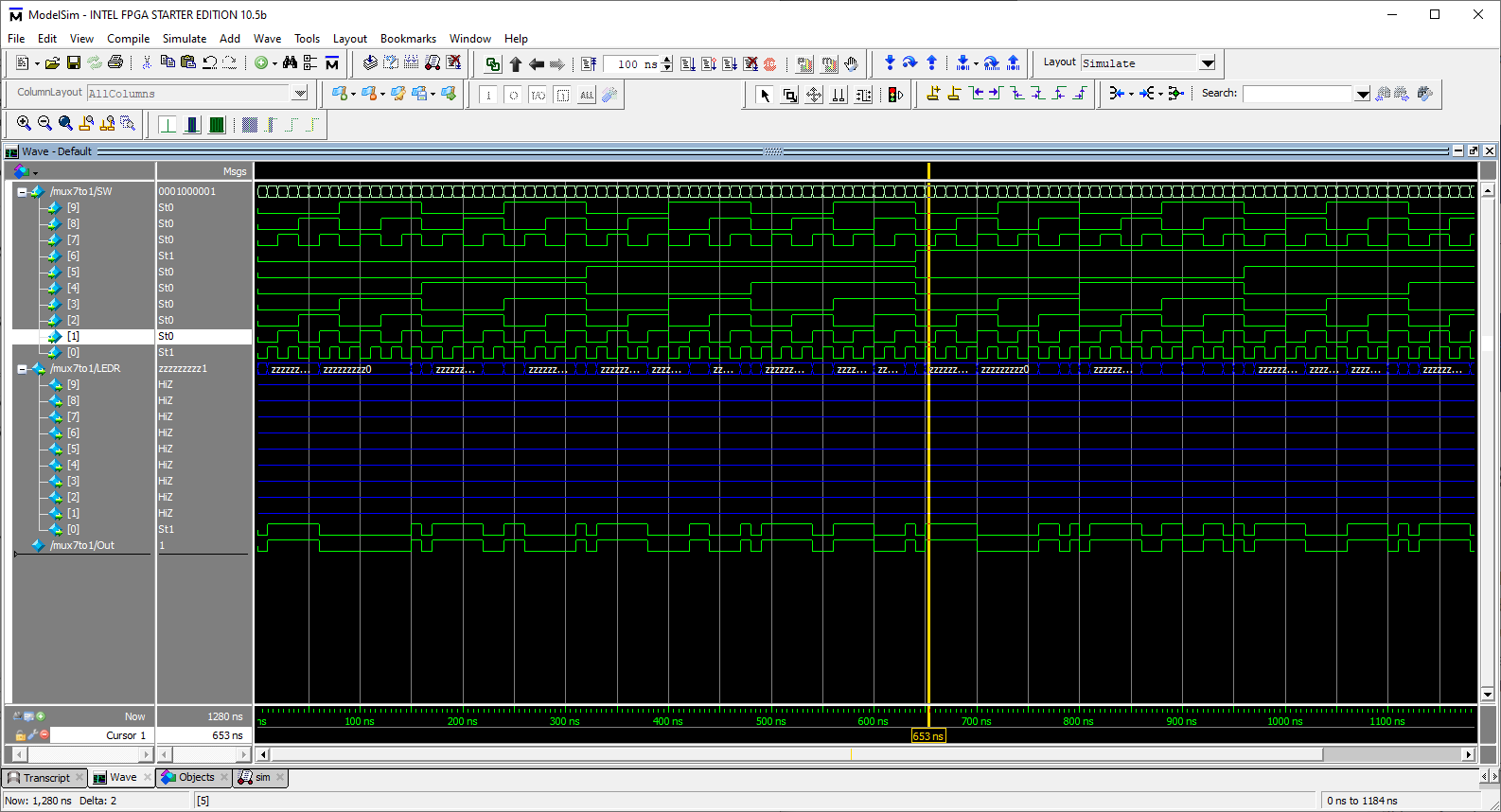
Lab 3 prelab

Part I:

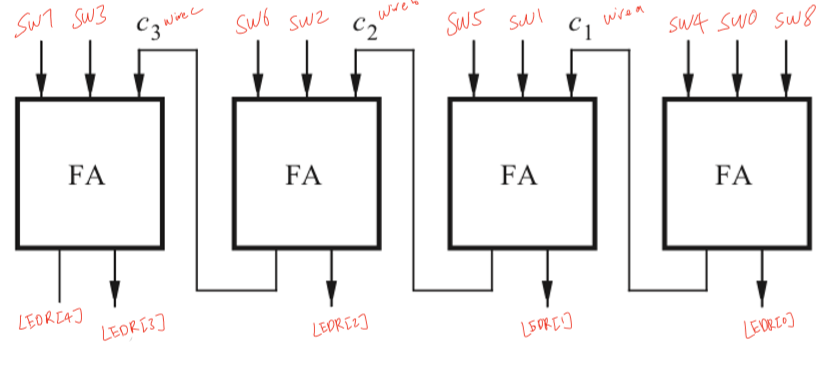
1. 

Schematic for 7to1 multiplexer

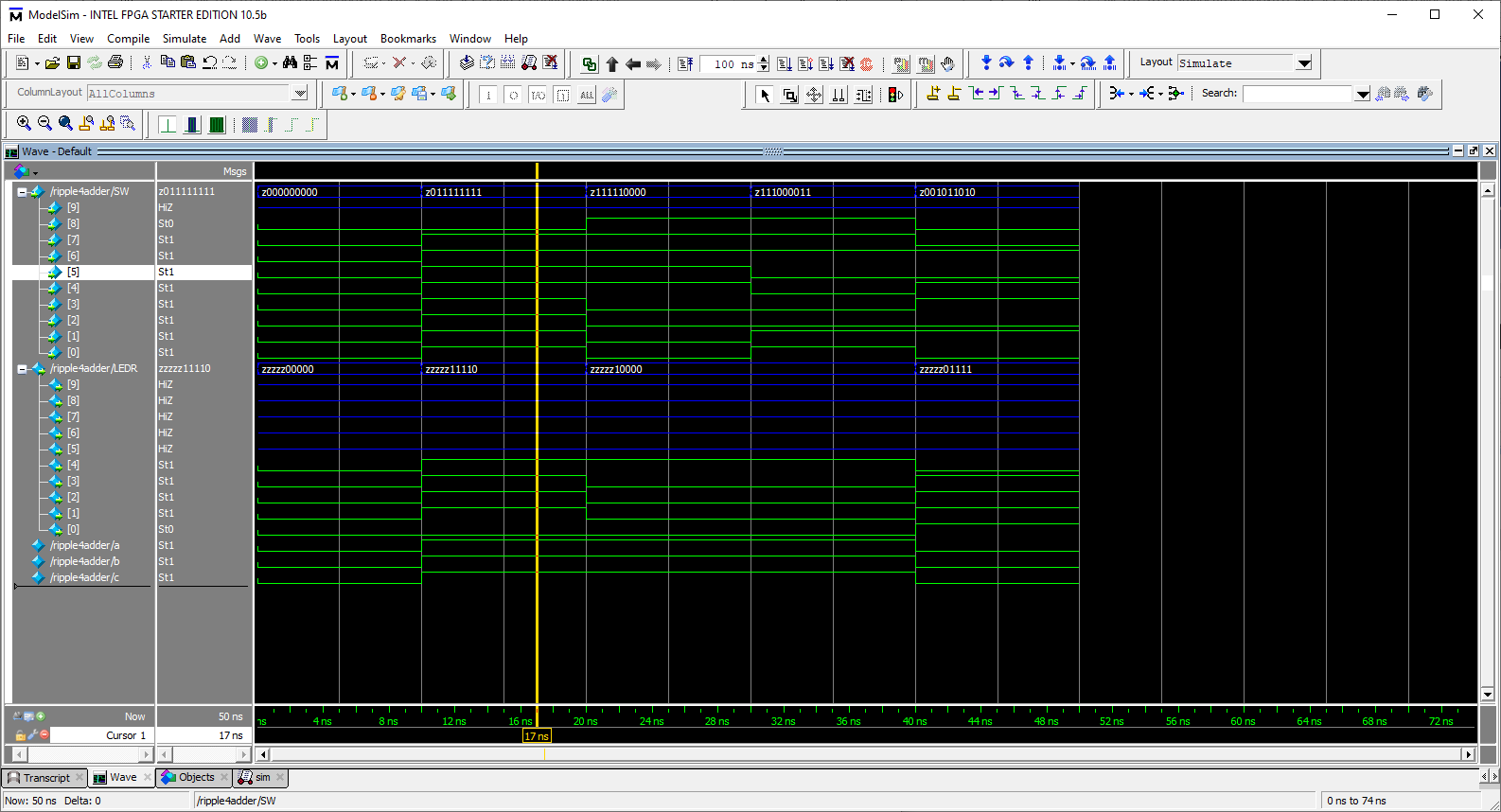
1. Submitted mux7to1.v on Quercus
2. 

Simulation of 7to1 multiplexer.

Part II:

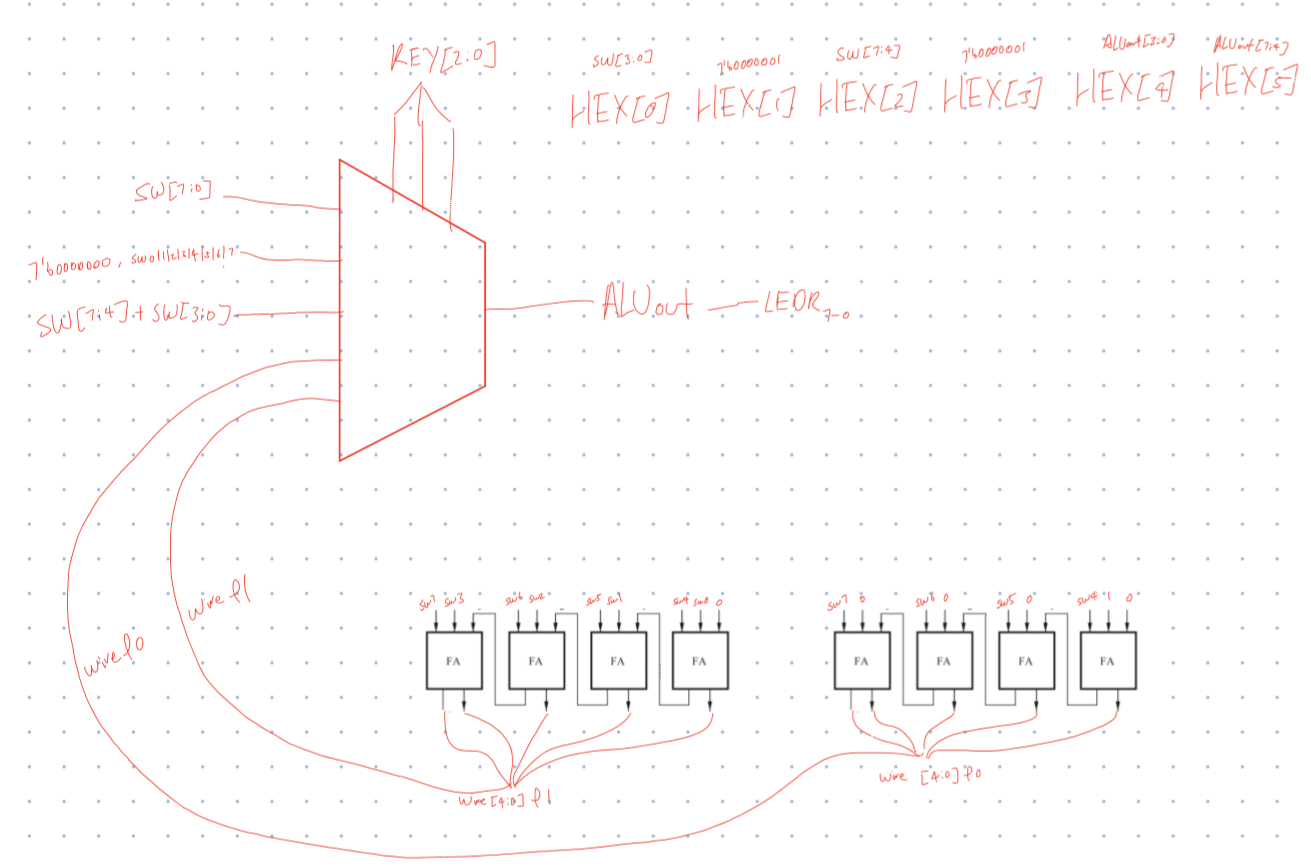
1. 

Schematic of 4-bit ripple carry adder

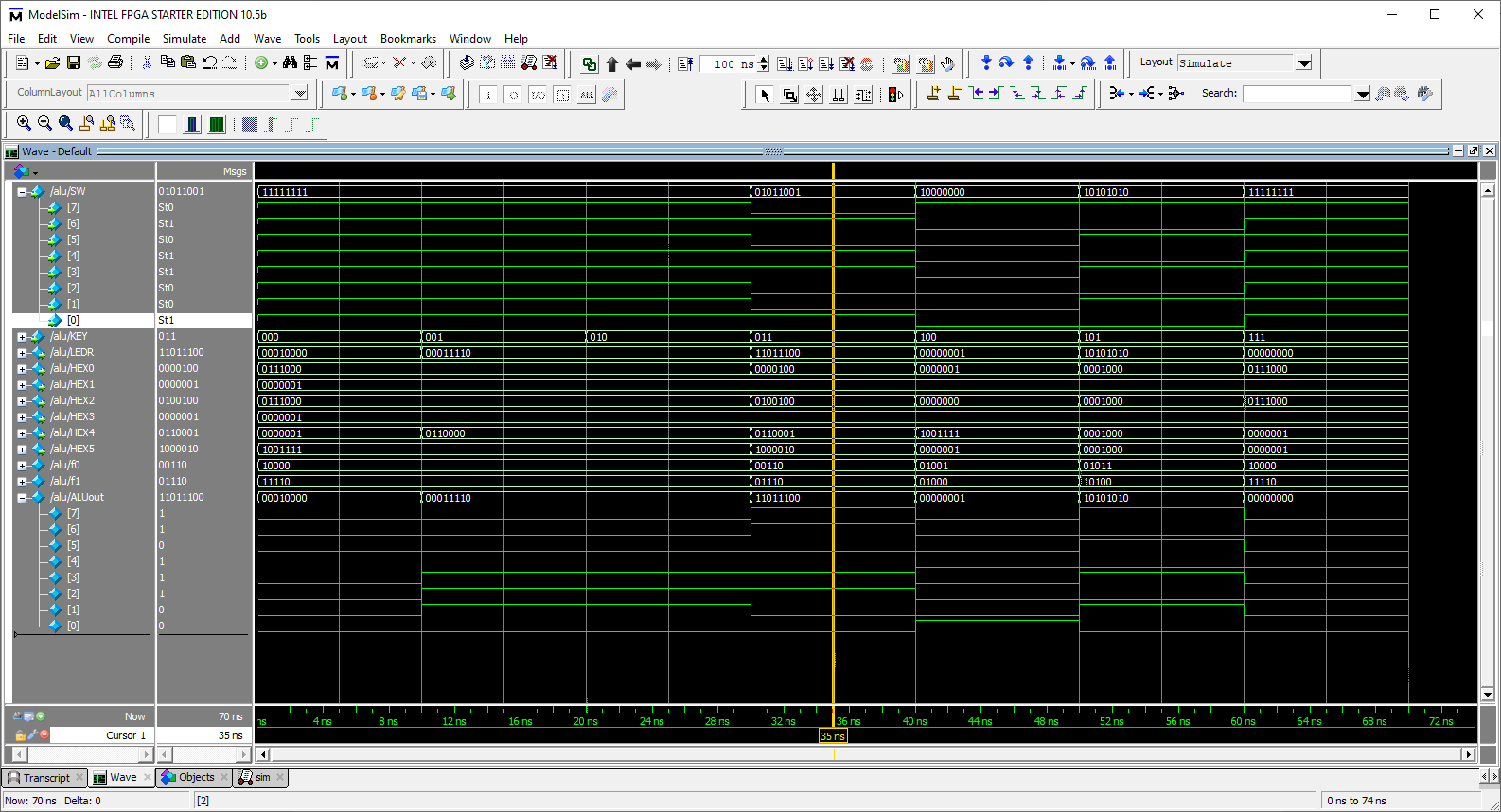
1. Verilog modules submitted on Quercus.
2. 

Simulation for 4-bit ripple carry adder. Test cases tested that the carry was working, and that circuit was not carrying unintentionally.

Part III:

1. 

Schematic for Arithmetic Logic Unit (ALU)

1. Code for ALU submitted on Quercus.
2. 

Simulation for ALU. All possible function cases tested, including default.